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1 Improving Java performance using hardware translation
Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John
June 2001 **Proceedings of the 15th international conference on Supercomputing**
Full text available: pdf(254.91 KB) Additional Information: full citation, abstract, references, citings, index terms

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

2 A survey of processors with explicit multithreading
Theo Ungerer, Borut Robič, Jurij Šilc
March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1
Full text available: pdf(920.16 KB) Additional Information: full citation, abstract, references, index terms

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors.A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

3 Architectures: 3D graphics LSI core for mobile phone "Z3D"
Masatoshi Kameyama, Yoshiyuki Kato, Hitoshi Fujimoto, Hiroyasu Negishi, Yukio Kodama, Yoshitsugu Inoue, Hiroyuki Kawai
July 2003 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware**
Full text available: pdf(649.83 KB) Additional Information: full citation, abstract, references

In this paper we describe the architecture of the 3D graphics LSI core for mobile phone

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L8	cpu and register and processor$ and ((translat$ or convert$) near5 instruction$) and (execut$ near5 java)	0	L8
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L5	((712/202 |712/36 |712/229)!.CCLS.)	487	L5
L4	L3 and l2	10	L4
L3	((717/136 |717/137 |717/138 |717/139 |717/140 |717/118 |717/143 |717/148)!.CCLS.)	716	L3
L2	cpu and register and processor$ and ((translat$ or convert$) near5 instruction$) and (execut$ near5 java)	51	L2
L1	cpu and register and processor and ((translat$ or convert$) near5 instruction$) and (exect$ near5 java)	0	L1

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